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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,265	03/12/2004	Tyler Lowrey	2024.46	7228

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Philip H. Schlazer
Energy Conversion Devices, Inc.
2956 Waterview Drive
Rochester Hills, MI 48309

EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,265	LOWREY ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7-9 and 16-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 7-9, 16-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7-9, and 16-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita (Us. 5,529,956) in view of Harshfield (US. 6,031,287).

Regarding claims 1, 7-8, 18, 20, 23, 30, 33, 41, 47 and 53, Morishita (Figs. 1A 1G) discloses a method of making an electrically contact element, comprising: providing a first dielectric layer 4, the first dielectric layer 4 having an opening, the opening having a sidewall surface and a bottom surface; forming a conductive layer 10 on the sidewall surface and the bottom surface (Fig. 1B); removing at least a portion of the conductive layer 10 from the bottom surface (Fig. 1D); forming a second dielectric layer 11 on the conductive layer 10 within the opening (also See Fig. 1D); and forming upper level wiring conductor 7 in electrical communication with the conductive layer 10.

Morishita does not disclose that the upper level-wiring conductor 7 is a phase-change programmable resistance material made of chalcogenide.

However, Harshfield (Fig. 24) teaches the forming of a phase-change programmable resistance material 130 of chalcogenide (column 7, lines 5-12 and column 14, lines 1-5) as an upper level-wiring conductor in electrical communication with a lower level-wiring conductor 106 through a conductive layer 124 (column 13, lines

48-51 and lines 66-67). Accordingly, it would have been obvious to modify the method of Morishita by forming the upper level wiring conductor 7 with a phase-change programmable resistance material because such a forming of the phase-change programmable resistance material for the upper level wiring conductor would provide a memory cell for a programmable memory device, as taught by Harshfield (column 14, lines 1-5).

Regarding claims 9, 29 and 39, Morishita does not disclose that the first dielectric layer 4 and the second dielectric 11 are formed of the same material.

However, Harshfield (Fig. 24) further teaches that the first dielectric 110 and the second dielectric layer 122 formed within the opening are formed of the same material (column 13, lines 45-47). Accordingly, it would have been obvious to form the first dielectric layer and the second dielectric layer with either the different material or the same material because the changing the materials of the first and second dielectric layers would not change the functions of the device.

Regarding claims 16, 21, 31, 42 and 48, Morishita further discloses that the forming conductive layer step comprises substantially conformally depositing the conductive layer 10 on the sidewall surface and the bottom surface (see Fig. 1B).

Regarding claims 17, 19, 22, 32, 40, 43, 45, 49 and 51, Morishita further discloses that the removing step comprises substantially anisotropically etching such as reactive ion etching (column 4, lines 19-23) to form a conductive sidewall spacer 10 (see Fig. 1D).

Regarding claims 24-28, 34-38, 44, 46, 50, 52 and 54-57, Morishita (Fig. 2) also discloses that the sidewall surface is the sidewall surface of the first dielectric layer 4, the second dielectric layer 12 is formed on the conductive layer 10 after the removing step (column 5, lines 10-15), and the second dielectric layer 12 is formed before the forming the upper level wiring conductor 7.

Response to Arguments

3. Applicant argues that it would not be obvious to combine Morishita with Harshfield because Fig. 25 of Harshfield does not suggest the upper level wiring being used as a chalcogenide memory material.

This argument is not persuasive because Fig. 24 of Harshfield is relied on for teaching the upper level wiring being used as a chalcogenide memory material, but not Fig. 25 as asserted by Applicant. Fig. 25 teaches that the layer 124 is used as a chalcogenide memory material. However, Fig. 24 is an alternative embodiment and teaches that the layer 124 is used as "an annular electrode" and formed by depositing a thin conductive film 118 made of conductive materials including titanium nitride, carbon, aluminum, etc. (column 13, lines 31-37 and lines 48-50). The thin conductive layer 124 is formed between the lower level wiring 106 and the upper level wiring 130 and functions as an interconnect for connecting the lower level wiring 106 to the upper level wiring 130, wherein the upper level wiring 130 is used as a chalcogenide memory material for memory element (column 14, lines 1-5). Therefore, Harshfield's Fig. 24 clearly suggests that the upper level wiring 130 is used as a chalcogenide memory material for a memory cell and is connected to the lower level wiring layer 106 through a

conductive layer 124 formed therebetween. Thus, in view of teaching of Harshfield's Fig. 24, one skilled in the art would motivate to substitute the upper level wiring 7 of Morishita with the upper level wiring 130 made of chalcogenide memory material in order to form a memory cell for a programmable memory device.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
May 28, 2006

PHAT X. CAO
PRIMARY EXAMINER